

Notice of Allowability

Application No.

09/103,873

Examiner

José R. Díaz

Applicant(s)

NAGANO ET AL.

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 9/8/04.
2. ☒ The allowed claim(s) is/are 1,4,6-10,29-31 and 33-38.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some* c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
- (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 1/30/01; 4/9/02.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Daniel Calder on September 16, 2004.

The application has been amended as follows:

Please cancel claims 11-27.

1. (Currently Amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate and including a lower electrode, a dielectric layer, and an upper electrode, said dielectric layer being formed from a ferroelectric material;

a first interlayer insulating layer provided so as to cover the capacitor;

a first interconnect selectively provided on the first interlayer insulating layer and electrically connected to the capacitor through a first contact hole formed in the first interlayer insulating layer;

a second interlayer insulating layer consisting of an interlayer insulating film having a tensile stress provided directly on the first interconnect; and

a second interconnect selectively provided directly on the second interlayer insulating layer and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating layer.

30. (Currently Amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate and including a lower electrode, a dielectric layer, and an upper electrode, said dielectric layer including a remnant polarization of approximately $10 \mu\text{C}/\text{cm}^2$;

a first interlayer insulating layer provided so as to cover the capacitor;

a first interconnect selectively provided on the first interlayer insulating layer and electrically connected to the capacitor through a first contact hole formed in the first interlayer insulating layer;

a second interlayer insulating layer consisting of an interlayer insulating film having a tensile stress provided directly on the first interconnect; and

a second interconnect selectively provided directly on the second interlayer insulating layer and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating layer.

31. (Currently Amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate and including a lower electrode, a dielectric layer, and an upper electrode, said dielectric layer including a remnant polarization of at least $10 \mu\text{C}/\text{cm}^2$;

a first interlayer insulating layer provided so as to cover the capacitor;

a first interconnect selectively provided on the first interlayer insulating layer and electrically connected to the capacitor through a first contact hole formed in the first interlayer insulating layer;

a second interlayer insulating layer consisting of an interlayer insulating film having a tensile stress provided directly on the first interconnect; and

a second interconnect selectively provided directly on the second interlayer insulating layer and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating layer.

33. (Currently Amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate having an integrated circuit thereon and including a lower electrode, a dielectric film, and an upper electrode, said dielectric film being formed from either a dielectric material having a high dielectric constant or a ferroelectric material;

a first interlayer insulating film provided so as to directly cover the capacitor;

a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a first contact hole formed in the first interlayer insulating film;

a second interlayer insulating layer consisting of an interlayer insulating film having a tensile stress provided directly on the first interconnect;

Art Unit: 2815

a second interconnect selectively provided directly on the second interlayer insulating layer and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating layer; [[and]]

a passivation layer provided so as to cover the second interconnect; and

a hydrogen supplying layer provided between the first interconnect and the second interlayer insulating layer excluding an area in which the capacitor is provided.

34. (Currently Amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate having an integrated circuit thereon and including a lower electrode, a dielectric film, and an upper electrode;

a first interlayer insulating film provided so as to directly cover the capacitor, the first interlayer insulating film having a tensile stress;

a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a contact hole formed in the first interlayer insulating film;

a second interlayer insulating layer consisting of an interlayer insulating film having a tensile stress provided directly on the first interconnect;

a second interconnect selectively provided directly on the second interlayer insulating layer and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating layer;

a passivation layer provided so as to cover the second interconnect; and

a hydrogen supplying layer provided between the first interconnect and the second interlayer insulating layer excluding an area in which the capacitor is provided.

Reasons for allowance

The following is an examiner's statement of reasons for allowance: the prior art fails to teach, disclose, or suggest, either alone or in combination, a semiconductor device comprising: a first interconnect selectively provided on the first interlayer insulating layer and electrically connected to the capacitor through a first contact hole formed in the first interlayer insulating layer; a second interlayer insulating layer consisting of an interlayer insulating film having a tensile stress provided directly on the first interconnect; and a second interconnect selectively provided directly on the second interlayer insulating layer and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Correspondence

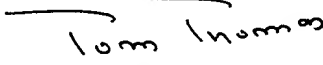
Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

Art Unit: 2815

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
9/16/04


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